FORZA

Single Slope ADC with On-chip Accelerated Continuous-time Differential Ramp Generator for Low Noise Column-Parallel CMOS Image Sensor

Dexue Zhang, Rami Yassine, Loc Truong, Jeff Rysinski,
Daniel Van Blerkom, Barmak Mansoorian

Forza Silicon Corporation, Pasadena, CA.

Contact: Dexue Zhang
2947 Bradley St, Suite#130
Pasadena, CA 91107

tel: 626-796-1182
fax: 626-796-5882
email: dexue@forzasilicon.com

Abstract: This paper presents a 12-bit single slope ADC architecture that uses an on-chip ramp generator for low noise column-parallel CMOS image sensor. An on-chip continuous-time ramp generator is used instead of a discrete-time implementation. This is to reduce the glitch noise caused by a high speed clocking of a discrete-time ramp. Differential topology is adopted to improve the power supply rejection (PSR) performance of the ramp generator. High speed ADC conversion is obtained with accelerated ramp signals by exploiting photon shot noise characteristics of image signals [1,2]. The ADC is designed to be highly scaleable and the architecture is used for a family of image sensors fabricated in TSMC 0.18um 3.3V/1.8V CMOS process. Measurements show a row noise of 13uV at gain 24x and 50uV at gain 3x. The total readout noise is 108uV at gain 24x and 171uV at gain 3x.

Figure 1 shows the differential column sample-and-hold, preamp and comparator using a topology described in [3]. The input stage allows differential kTC noise cancellation for increased PSR. And a front-end auto-zero phase allows the use of a high-gain preamp to reduce column fixed-pattern noise.

Figure 2 shows the diagram of the accelerated continuous-time differential ramp generator. The accelerated ramp generator is used to increase the 12-bit ADC conversion rate. In order to obtain the binary increasing slope of the ramp signals, Iint is seeded by a 2-bit current DAC. Each DAC bit doubles the integrating current. A super current source is designed to generate the currents to reduce mismatch, increase output impedance and eliminate glitches. This approach succeeds in meeting the 0.1% mismatch requirement between the slopes of the ramp signals across PVT corners. In order to create a knee as ideal as possible when the slope is changed and to reduce the knee's sensitivity to PVT corners, a local feedback circuit is added around the current sources.

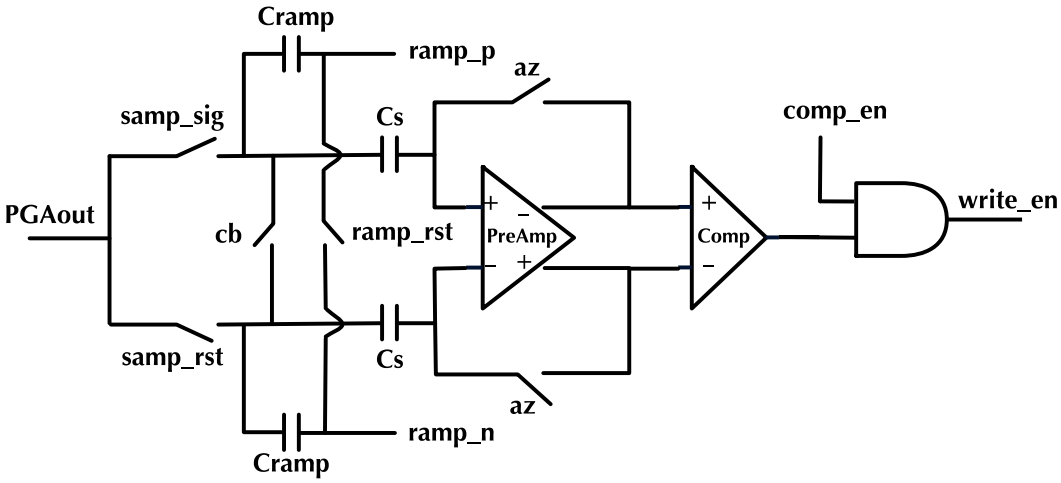

Figure 1. Block Diagram

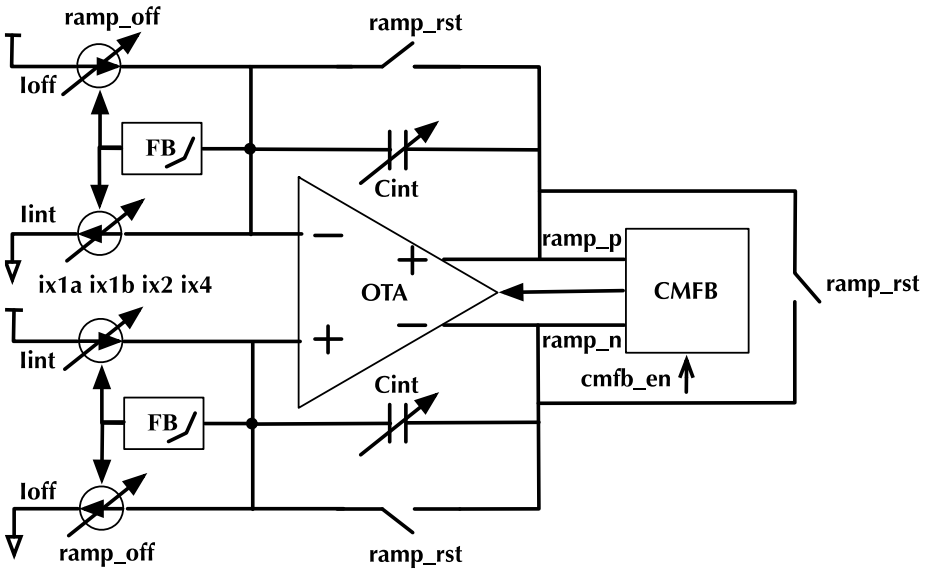

Figure 2. Ramp generator diagram

References:

[1] Toshinori Otaka, et al., "12-Bit Column-Parallel ADC with Accelerated Ramp", IISW, 2005.

[2] M.F.Snoeij, et al., "A Low-Power Column-Parallel 12-bit ADC for CMOS Imagers", IISW, 2005.

[3] Daniel Van Blerkom, "Column parallel readout with a differential sloped A/D converter", US Patent No.7.471.231.82, 2008.