

BSI Low Light Level CMOS Image Sensor Employing P-type Pixel

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Abstract - A backside illuminated (BSI) CMOS imager technology optimized for night vision applications (NV-CMOS™) has been developed employing a hole-based p-type pixel (pMOS). Benefits of the technology include lower dark current and reduced random telegraph noise (RTN) as compared to conventional electron-based n-type pixels (nMOS). The measured performance of the BSI first generation digital reference design is reported. A high definition sensor (1920 x 1200) now in development is described.

1. INTRODUCTION

Low light level imaging at night in quarter moon and below imaging conditions with a un-intensified silicon sensor requires proper selection and optimization of imager design features. First, backside illumination with relatively thick silicon is desirable to collect the photons over the visible and near-infrared spectrum, particularly at wavelengths above 800 nm to gather the night glow photon flux. Second, a pixel size in the 5-8 μm range is desirable for light gathering, dynamic range and optics design considerations. Third, the readout temporal noise needs to be reduced to < 2 carriers RMS (median) with a tight noise distribution if one wants to operate in the pixel size range identified with roughly f1.5 optics at 60 frames per second. Fourth, the dark current needs to be reduced to the point that the dark current shot noise is below the readout temporal noise at the maximum operating temperature of the imager. For low power applications, which cannot permit thermoelectric cooling, this can drive the dark current requirement to values in the range of 20 pA/cm² at up to 60 C imager temperature. Fifth, to achieve discrimination capability at high range distances it is desirable to maintain high modulation transfer function (MTF) spatial modulation at Nyquist. Other design considerations include fixed pattern noise (FPN) reduction to levels below the temporal noise, imager format size optimized for field of view and power dissipation, and techniques for extended dynamic range. The work described in this paper is the design solution for our NV-CMOS™ sensor technology.

2. CHOICE OF THE P-TYPE (pMOS) PIXEL

The pMOS pixel was selected for our low light imaging work. The pixel design is shown in Figure 1. It is based upon the nMOS pixel work that SRI has been refining over the past few years for scientific and aerospace applications [1]. The technology has been radiation hardened for space applications such as the 16 Mpixel focal plane for the SoloHI mission to the sun [2]. Both

the n-type and p-type pixel technologies are fabricated in a 0.18 μm CMOS technology at TowerJazz, Newport Beach, California.

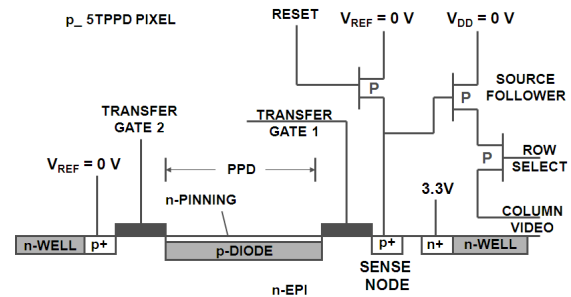


Figure 1. p-type pixel (pMOS) on n-epi optimized for BSI.

The baseline pMOS pixel is a 5T pinned photo-diode (PPD) design built on n-type epi with a 8 μm pixel size. The second transfer gate is used for sub-frame integration time control and dynamic range control. Since this is a hole-based pixel, the video is inverted as are the control signals, as compared to the nMOS pixel technology.

A primary advantage of the pMOS pixel compared to the nMOS pixel is the lower dark current (Figure 2), as reported in the literature [3, Kodak].

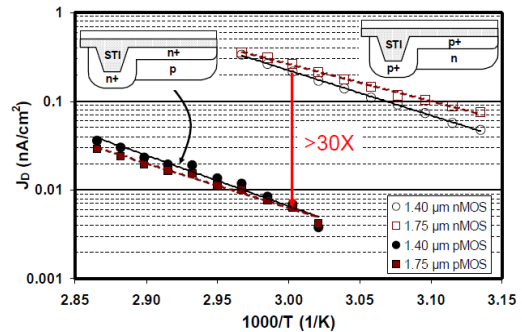


Figure 2. pMOS pixel vs. nMOS pixel measured dark current showing up to 30X reduction with the pMOS pixel compared to the nMOS pixel in the same foundry (Ref: Stevens, Kodak).

Our development efforts over the past three years have resulted in the understanding of a number of other advantages of the pMOS pixel compared to the nMOS pixel, beyond the lower thermal dark current. The pMOS pixel also offers 1.) lower RTN, 2.) less TG leakage current, 3.) greater tolerance to high energy damaging radiation sources, 4.) impact ionization is less for holes than electrons which is important for luminescence issues, and 5.) more flexibility in engineering a reliable sense

node. A drawback of the pMOS pixel is the lower mobility of holes compared to electrons, which effects the transfer gate speed and the drive capability of the pixel source follower. Our experience has been that we can engineer designs to accommodate these negative aspects of the technology.

A comparison of the pMOS pixel and the nMOS pixel noise histograms is shown in Figure 3. The histograms are developed from individual noise levels from a row of 256 pMOS and nMOS pixels with the same architectural features. The conversion per carrier is 0.2 carriers / DN for both pixel types. The ‘background’ noise is fitted with a Gaussian curve to show the RTN skirts more clearly. The pMOS pixel displays considerably lower RTN than the nMOS pixel.

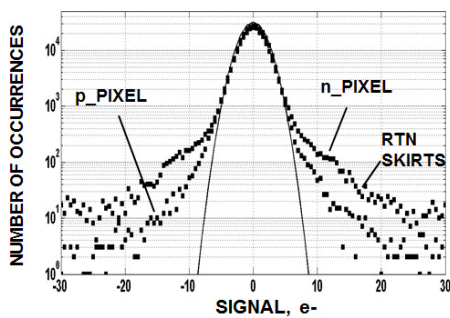


Figure 3. pMOS pixel vs. nMOS pixel noise histograms. The data is for pixels with the same architectural features. The pMOS pixel shows a lower RTN skirt.

Work is continuing on the design and process optimization of the pMOS pixel source follower for lowest noise. Figure 4 shows an early result for an experimental pixel with a 111 uV/h+ source follower conversion gain and a 1.4 h+ RMS noise at a 24 usec row rate. The goal is to achieve this noise floor at the 12 usec row time required for the HD imager and at a lower conversion gain to provide more sense node-determined pixel dynamic range.

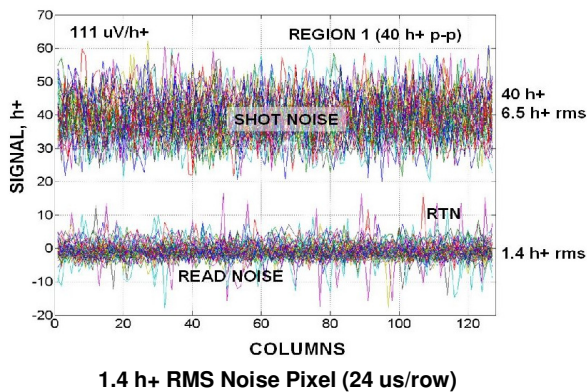


Figure 4. Gen I measured pixel noise (1.4 h+ RMS) with 111 uV/h+ conversion gain.

3. DIGITAL REFERENCE DESIGN

A digital reference design was reported in March 2012 [4]. The reticle included the reference design and a number of pixel test arrays. The architecture for the digital reference design is shown in Figure 5.

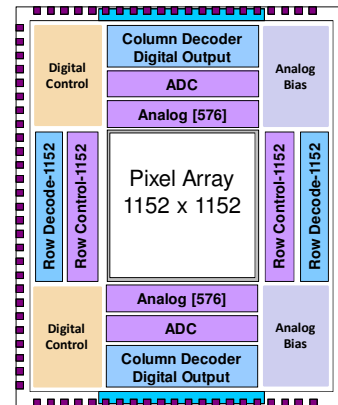


Figure 5. NV-CMOS reference imager architecture. This digital sensor was used for BSI demonstrations.

The NV-CMOS reference design incorporates column parallel correlated double sampling processors with front-end gain, an extended dynamic range operating mode and column parallel 12-bit analog-to-digital converters. The design was optimized for low noise while focusing on achieving low power dissipation.

4. REFERENCE DESIGN PERFORMANCE

The NV-CMOS reference design was fabricated using n-type epi on SOI wafers. The epi was 8 um thick and engineered for high MTF performance. The measured performance is discussed in this section.

The imaging performance of a 640 x 480 VGA pixel test area within the 1152 x 1152 pixel array is shown in Figure 6. The pixel in this test area has a conversion gain of 80 uV/h+. This is a backside illuminated imager which employed wafer scale thinning. There is no non-uniformity or defect correction for this image.

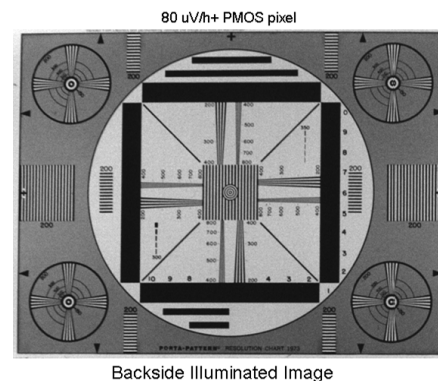


Figure 6. BSI digital reference design imaging performance. Wafer scale thinning employing SOI starting material.

The reference design has an extended dynamic range mode which is demonstrated in Figure 7. The top image was taken in the linear readout mode with no dynamic range extension. The bottom image was taken in the extended dynamic range (XDR) mode. The test pattern is back illuminated. A lamp filament is projected onto the front of the test pattern using a microscope lens. In the XDR mode the test pattern “300” can be seen as well as the gray scale of the unsaturated filament image.

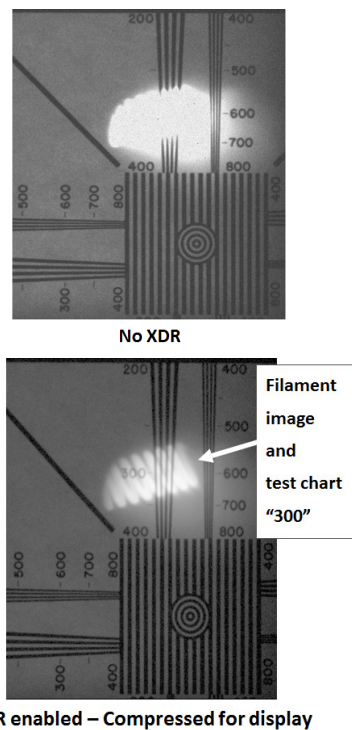


Figure 7. Demonstration of extended dynamic range (XDR).

The 12 bit ADC performance for DNL and INL is shown in Figure 8. The matching between the column ADCs has been very good providing high quality images without off-chip correction. For optimum imaging performance, particularly at low light levels, off-chip non-uniformity correction (NUC) will be employed.

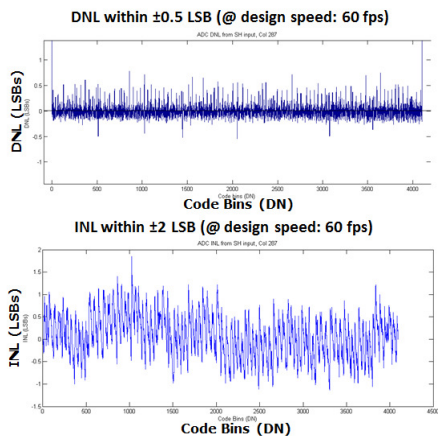


Figure 8. Measured DNL of the ADC of +/- 0.5 LSB. Measured INL of the ADC of +/- 2 LSB.

The measured quantum efficiency for the Gen I and Gen II wafer scale BSI process are shown in Figure 9. The Gen I process (red curve: MSS paper, 8 um Si) has a limited anti-reflection coating (ARC). The Gen II process (New SRI Measured, 8 um Si) has a multi-layer ARC optimized for broadband response. Both processes were applied to the same type of SOI wafer/process split from the same first wafer lot of the reference design. The simulated Gen II QE (8 um Si) is shown in the figure, as is the simulated Gen II QE on a 16 um thick epi (Projected, 16 um Si).

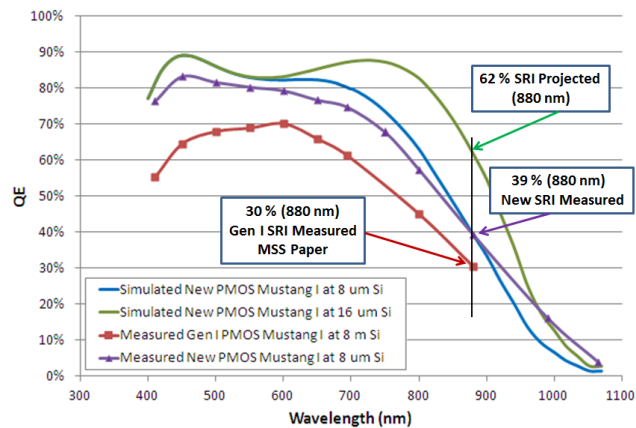


Figure 9. Measured quantum efficiency (QE) for the Gen I process and the Gen II process (New SRI Measured). Simulated Gen II ARC on 8 um epi and on 16 um epi.

The measured MTF on the 8 um epi starting material with the Gen I ARC is shown in Figure 10. The MTF data was measured on the same imager, which produced the Gen I quantum efficiency curve shown in Figure 9. The MTF curve was measured at 650 nm using calibrated sinewave patterns and calibrated optics. The results are in good agreement with our MTF simulations.

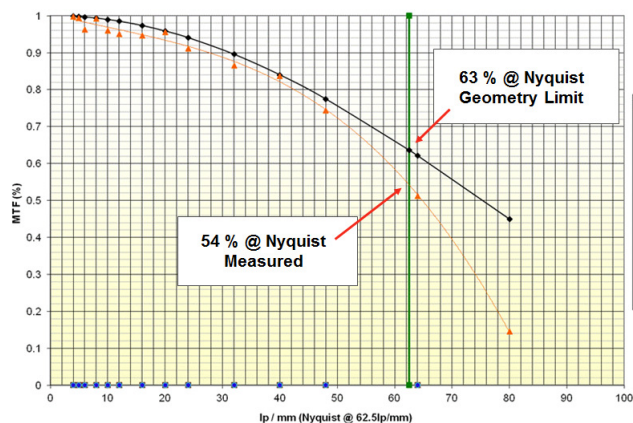


Figure 10. Measured backside illuminated MTF at 650 nm for Gen I process. The pixel is 8 um and the epi is 8 um. Geometry limited MTF for 100 % fill-factor also shown.

The measured Nyquist MTF at 650 nm is 54 %. This performance is achieved with an engineered epi/wafer fab process which quickly sweeps the photocarriers into the

charge storage region of the pinned photo-diode. With 650 nm illumination, nearly 50 % of the holes are created within the first 2 um of the 8 um epi. An optimized epi and process is required to achieve the high MTF.

The measured readout temporal noise at the digital output of the imager reported here (80 uV/h+ pixel) at a 12 us row rate (12 us row rate needed for full HD design at 60 fps) is 4 h+ RMS (median). New pixel designs and process improvements are on-going to drive this down to the target of 1.5 h+ RMS (median).

The measured dark current for the 8 um epi at 27 C is 150 pA/cm² for the imager reported here. The reference design wafer lot did not have the full pMOS pixel process optimization. New wafer lots have been run showing dark current reduction toward the target of 20 pA/cm² at nominally 50 C.

5. HD SENSOR DEVELOPMENT

The 1920 x 1200 high definition (HD) sensor design is nearing completion. First BSI versions of the design will be in test Q4 of 2013. The performance of the new sensor is expected to be similar to that of the reference design, with enhancements being lower readout noise and lower dark current from the process optimizations that have been underway during 2012 and 2013.

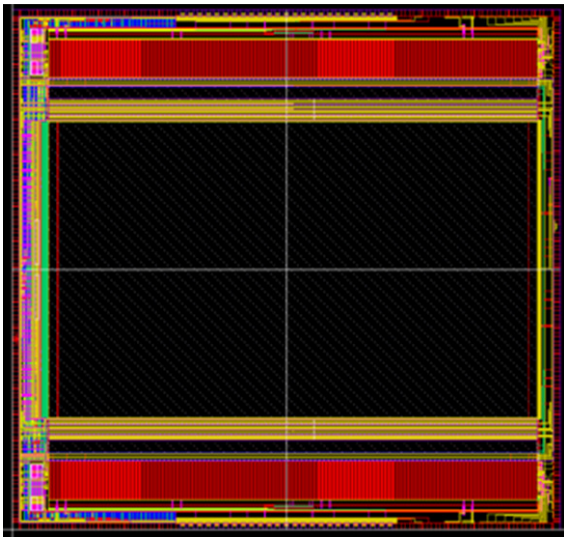


Figure 11. BSI CMOS 1920 x 1200 pMOS pixel digital sensor layout (pixel array removed: 8 um pixel). Designed for rolling shutter operation (60 fps) and snapshot operation (30 fps).

The 1152 x 1152 reference imager and the scaled-up HD sensor have been developed to minimize power consumption. Measured power consumption of the reference imager and projected power consumption of the HD sensor are shown in Table 1. The 1920 x 1200 HD sensor running at 60 fps is projected to dissipate 400 mW.

Imager Subsection	1K x 1K Reference Imager		HD Sensor
	Estimated Power (mW)	Measured Power (mW)	Estimated Power (mW)
Pixel Bias and Row Control	31.86	41.98	71.54
Analog Signal Chain with ADC	64.76	70.58	125.51
High Speed I/O	87.00	79.44	96.72
Digital Control	34.60	34.40	51.66
PLL			20.64
Analog Bias			18.00
Temperature Sensor			9.00
Total Power	218.22	226.40	393.07

Table 1. Measured power dissipation of the reference design and projected power dissipation of the 1920 x 1200 HD design running at 60 frames per second, progressive scan.

6. CONCLUSION

A backside illuminated (BSI) CMOS imager technology optimized for night vision applications (NV-CMOSTM) has been developed employing a hole-based p-type pixel (pMOS). The pMOS pixel technology was selected for its lower dark current and reduced RTN as compared to the nMOS pixel technology. When fully optimized the technology promises to provide a very attractive approach to achieving solid state low light imaging for multiple application areas.

REFERENCES

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