Analysis and Simulation of CTIA-based Pixel Reset Noise

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ABSTRACT

This paper describes an approach for accurately simulating the reset noise of CTIA-based pixels. Using a circuit simulator to find the reset noise of a CTIA based pixel is not straightforward, due to the noise sampling and charge re-distribution after the reset switch opens. This often leads to an equation-based analysis of the pixel noise, which is cumbersome for actual design work and incompatible with a mixed-signal design flow for advanced ROIC designs.

In a CTIA-based ROIC, the start of pixel integration is defined by the opening of the CTIA reset switch. The opening of this switch down-converts the wideband noise of the circuit to DC, and the charge is then redistributed by the CTIA to create an output reset noise. This reset noise can be removed by correlated double sampling (CDS). However, it is important to understand the magnitude of the reset noise in order to evaluate the effectiveness of the CDS scheme. CDS can be performed either in the pixel, or externally in the analog or digital domains. The specifications of the signal chain depend on the amount of reset noise and the degree of cancellation required.

Simulation of the reset noise in SPICE is not straightforward, since the charge is redistributed after the switch opens, and the noise on the two capacitors is correlated and cannot be treated independently. We describe a simulation technique that gives accurate estimates of the pixel reset noise, and verify the results using Spectre-RF.

Keywords: CTIA, ROIC, Focal Plane Array, Reset Noise

1. INTRODUCTION

Infrared sensors are steadily increasing in functionality and integration, as designers take advantage of advanced CMOS technologies for the implementation of readout integrated circuits (ROIC). Fine line CMOS enables tighter integration of the pixel circuitry, driving pixel sizes down. In addition, modern processes allow high-speed readout electronics to be designed for faster frame rates. Detector materials are also improving, with lower capacitance and dark current. In a parallel to the advances taking place in CMOS visible image sensors, high resolution, high speed infrared imagers put pressure on the sensor noise performance to maintain or improve the signal to noise (SNR) as the integrated charge per pixel decreases.

The charge transimpedance amplifier (CTIA) based pixel is a popular choice for high sensitivity infrared ROIC designs. It offers superior linearity and low frame-to-frame lag compared to other direct-injection (DI) pixel designs, while maintaining tight control on the photodiode bias point to reduce dark current. Both DI and CTIA pixels exhibit reset noise; however, the reset noise on CTIA pixels is complicated by the additional reset switch noise left on the input capacitance, and the noise of the transimpedance amplifier. Most analyses of CTIA operation ignore the reset noise, since it is assumed to be perfectly cancelled with correlated double sampling (CDS). However, it is important to understand the magnitude of the reset noise and its implications to the system performance, and how it can be reduced, since other non-idealities in the system can reduce the effectiveness of CDS.

The first section of this paper reviews the CTIA pixel operation and motivates the investigation of the CTIA reset noise. The next section presents a mathematical analysis of the reset noise, under a simplifying assumption that allows for closed form noise expressions. The last section describes a simulation methodology for simulating the reset noise using a standard Spice AC Noise simulation, and compares the results with much more computationally intensive simulations using SpectreRF (a simulation tool for cyclostationary noise) and transient noise simulations (a relatively new technique which introduces device noise stimulus into transient simulations).

2. CTIA OPERATION & NOISE

A typical CTIA pixel schematic is shown in Figure 1. A CTIA pixel works as follows: prior to the start of integration, the feedback capacitance is cleared of charge with a reset switch. Then the reset switch is opened to begin integration, at which point the amplifier integrates the charge from the detector onto the feedback capacitor. Within the output range of the amplifier, the CTIA pixel output voltage is a linear function of the integrated charge, while the input node is kept at a voltage near its reset voltage level through the negative feedback of the circuit.
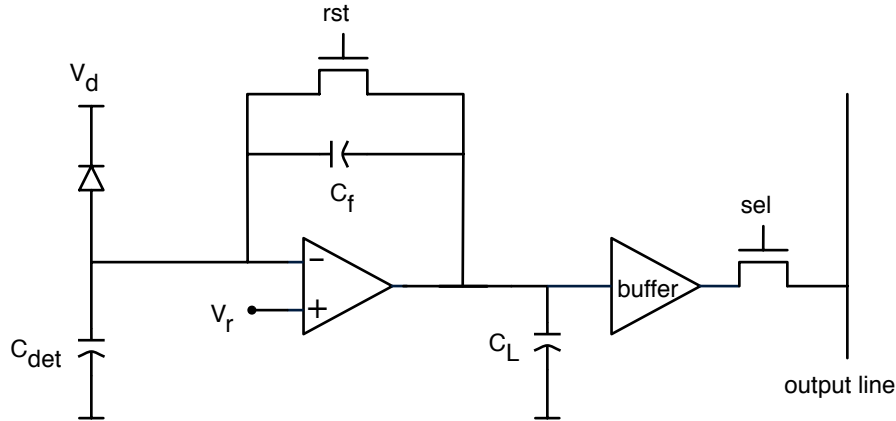

Figure 1 – A typical CTIA-based pixel schematic; in this example, the CTIA output is buffered before being driven onto the output column bus.

The output from a CTIA pixel through multiple reset and integration cycles is sketched in Figure 2. The CTIA settles to a different starting point after each reset completes. The reset noise is this uncertainty in the voltage level just after the reset switch has opened. It can be cancelled through CDS, which involves reading the pixel twice – once at the beginning of the integration time, and once at the end; and so it is mostly ignored in the noise analysis of CTIA pixels in the literature. [1],[2],[3]
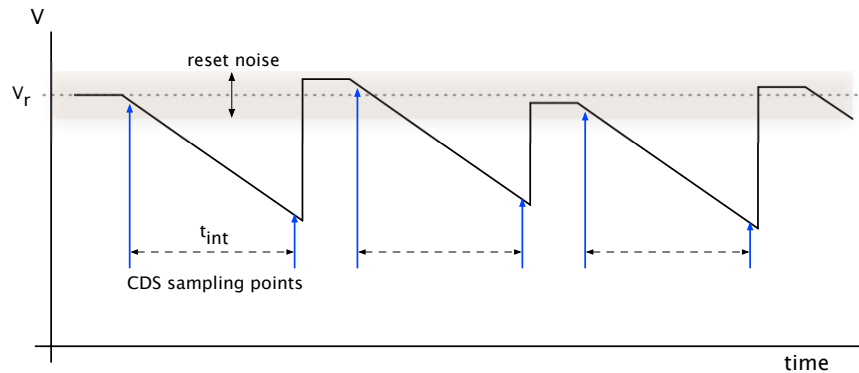

Figure 2 – Sketch of a CTIA pixel output under constant illumination for multiple reset and integration cycles. V_r is the mean reset level. Also shown are the CDS sampling points, when CDS is applied to the output. (After [1])

However, applying CDS requires additional complexity in the form of a frame memory and the circuitry to subtract the two samples from each other. Digital CDS performs this subtraction after ADC conversion of the two CDS samples. In this case, a digital frame memory is required to store the first sample, which is subtracted when the second sample is obtained and converted. Digital CDS also means that the ROIC analog signal chain and ADC must operate at twice the line rate, in order to obtain a first CDS sample and a second CDS sample (at a different row) in one line time. To determine the improvement provided by CDS requires comparing the reset noise with the noise levels of the rest of the system and the readout speed/noise tradeoffs. Knowing the magnitude of the reset noise also allows the designer to allocate an appropriate subset of the full bit resolution to the first CDS sample, reducing the frame memory required.

In-pixel CDS is an alternative approach, where the frame storage is an analog memory in the pixel. Since this analog memory has its own kTC noises, it is important to compare this noise with the reset noise to ensure that the cancellation will be effective.

Finally, the reset noise can be used as an additional measurement to characterize the CTIA pixel operation and verify the detector capacitance.

3. RESET NOISE ANALYSIS

Analysis of the reset noise of the CTIA pixel is complicated by the fact that the total charge left on the input node when the reset switch is opened is stored on two different capacitors. The noise analysis must take this into account by performing the noise integrals in the charge domain. The total charge on the input node is the sum of the charge on the input and feedback capacitors:

$$q_x = C_s v_x + C_f(v_x - v_o) \tag{1}$$

C_s is the input capacitance, including the capacitance of the detector, amplifier and parasitics, and C_f is the feedback capacitance, which includes the drawn feedback capacitance and any parasitics from the amplifier devices and wiring.

There are two dominant noise sources in the circuit – the thermal noise of the reset switch resistance, and the thermal noise of the amplifier. As these two noise sources are uncorrelated, we can treat them independently and add the results in rms.

The small signal equivalent circuit for noise analysis is shown in Figure 3. For simplicity, we assume the amplifier output resistance is high enough that it can be ignored for the frequency range of interest.
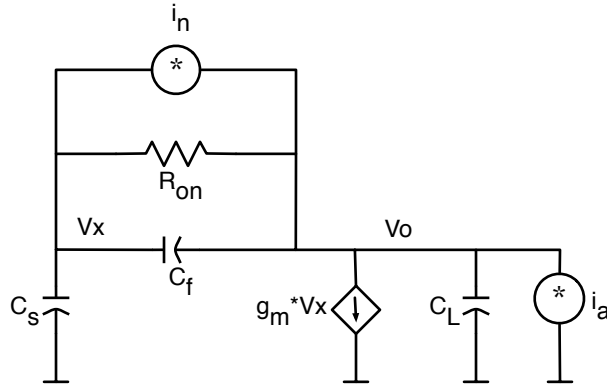

Figure 3 – Small signal equivalent circuit for noise analysis.

For the reset resistor thermal noise, the transfer function from the resistor noise current to total charge is

$$H_n(s) = \frac{R_{on} g_m C_f + s(C_s C_L + C_f C_L + C_f C_s)}{s^2 R_{on}(C_s C_L + C_f C_L + C_f C_s) + s(R_{on} g_m C_f + C_L + C_s) + g_m} \tag{2}$$

where R_{on} is the on resistance of the reset switch, and g_m is the transimpedance gain of the amplifier. For the amplifier thermal noise, the transfer function is

$$H_a(s) = \frac{C_s}{s^2 R_{on}(C_s C_L + C_f C_L + C_f C_s) + s(R_{on} g_m C_f + C_L + C_s) + g_m} \tag{3}$$

The one-sided noise current power spectral density (PSD) in units $\left(\frac{A^2}{Hz}\right)$ from the reset resistor and amplifier are

$$S_n(f) = \frac{4kT}{R_{on}} \tag{4}$$

and

$$S_a(f) = 4kT\gamma g_m \alpha \tag{5}$$

In the amplifier noise current PSD, $\gamma = \frac{2}{3}$ classically, but for modern short-channel processes it is between 1 and 1.5. The term α is included to model the additional noise contribution of the load device, and is $\left(1 + \frac{g_{mp}}{g_{mn}}\right)$.

Making the assumption that $R_{on} = \frac{1}{g_m}$, the noise integrals can be computed analytically (using, for example, the sum of residues approach described in [2])

$$\overline{q_n^2} = \int_0^\infty S_n(f)|H_n(s)|^2 \, df = kT\left(C_f + \frac{C_s C_L}{C_L + C_s + C_f}\right) \tag{6}$$

and

$$\overline{q_a^2} = \int_0^\infty S_a(f)|H_a(s)|^2 \, df = kT\gamma\alpha\left(\frac{C_s^2}{(C_L + C_s + C_f)}\right) \tag{7}$$

The total reset noise charge can then be written:

$$\overline{q_T^2} = kT\left(C_f + \frac{C_s C_L}{(C_L + C_s + C_f)} + \frac{\gamma\alpha C_s^2}{(C_L + C_s + C_f)}\right) \tag{8}$$

The total noise charge consists of three terms; the first two terms originate from the reset switch and the last term comes from the amplifier noise. The first term is the kTC noise of the feedback capacitor. If the feedback capacitor is small compared to the other capacitors, the second term reduces to the kTC noise of the parallel combination of the input capacitance and the load capacitance. The third term is essentially the amplifier noise appearing across the input capacitance.

In many cases, the detector and feedback capacitances are fixed by the parameters of the imaging system. The detector material and the pixel area determine the detector capacitance, while the desired conversion gain and full-well determine the feedback capacitance. The load capacitance can be adjusted, however, depending on the area available in the CTIA pixel. If $C_f \ll C_s, C_L$ then for $C_L > \gamma\alpha C_s$, the kTC noise of the reset switch dominates the total reset noise, whereas otherwise the amplifier noise dominates the total reset noise. (Note that as shown in [5] for a different circuit topology, the relative noise contributions also depend on the product of R_{on} and g_m.)

Increasing the load capacitance can lower the reset noise, by lowering the bandwidth of the amplifier and reducing its noise contribution. However, this also increases the length of time required for the CTIA to settle to the reset value. In addition, the incremental improvement in the noise decreases for large load capacitances. This can be seen from Figure 4, where contours of C_L vs. C_S are graphed that achieve different constant reset noise levels in electrons.

The assumption that $R_{on} = \frac{1}{g_m}$ is not totally unreasonable for a CTIA pixel, especially one used in a high-resolution array. The CTIA amplifier device sizes are restricted due to the pixel size, while the bias current must also be low to limit the power dissipation and IR drops in the array. The reset switch is typically made as small in width as possible, to minimize the clock feed-through and charge injection that creates a voltage pedestal when the reset switch is opened. On the other hand, the reset switch length is increased over the minimum to avoid leakage through the switch. All this combines to make the reset switch R_{on} relatively high and the amplifier g_m small. The example design used in the next section is based on 3.3V 0.18um device models, and is shown in Figure 5. In this circuit the amplifier device M1 W/L is 6um/1um, and the reset switch Mr W/L is 0.8um/1um. With 3uA of bias current, this leads to g_m=34uS and R_{on}=30Kohms, which satisfies the analysis assumption.
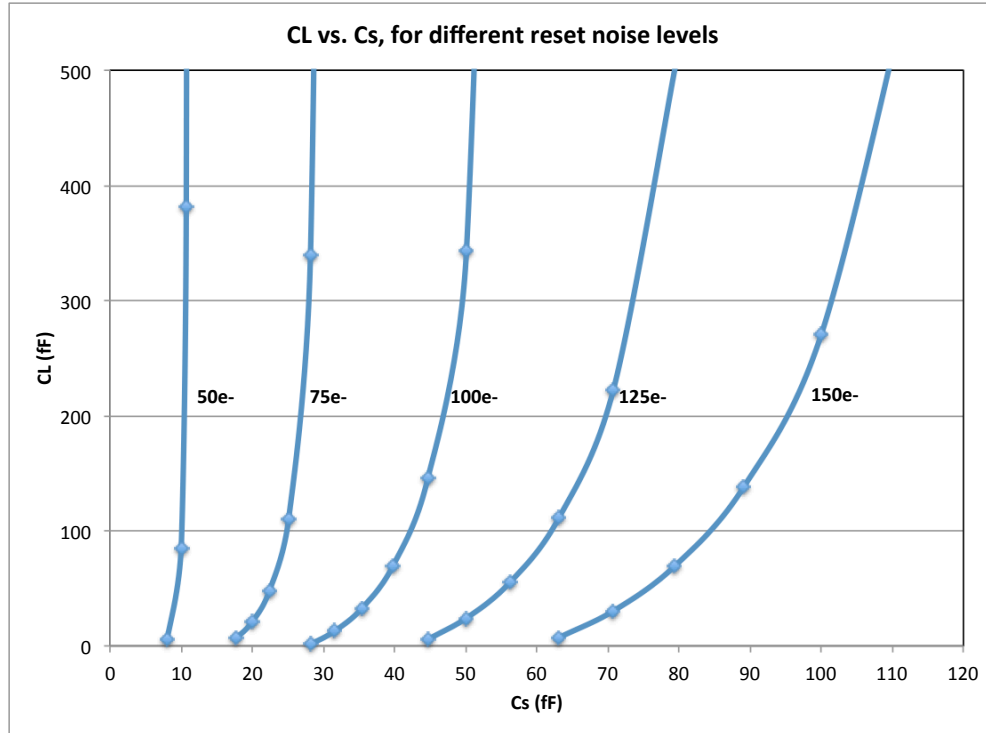
Figure 4 – Contours of constant reset noise levels in electrons, for combination of values of C_s and C_L. Here, $C_f = 5fF$, $\gamma = 1.4$ and $\alpha = 1.8$.

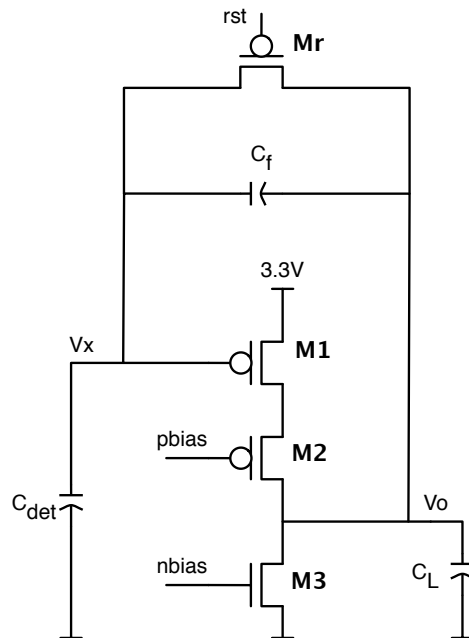Figure 5 – CTIA pixel schematic used in the simulations. For a 3 uA bias current, the amplifier $g_m = 34$ uS, and the reset switch $R_{on} = 30$ Kohms – this satisfies the assumption made in the analysis above that $R_{on} = 1/g_m$, so that the simulation results can be compared with the analysis results. The input capacitance of the amplifier was ~25fF. The noise of the devices and amplifier is such that $\gamma = 1.4$ and $\alpha = 1.8$.

4. RESET NOISE SIMULATION

The analysis above is valuable for an initial estimate of the reset noise; but to predict the actual performance in silicon, circuit simulations with the device models are necessary. A critical verification step in modern mixed-signal design flows is the parasitic extraction of the final layout, followed by simulation with the extracted parasitics. This is especially important for the CTIA based pixel, since the performance is sensitive to the parasitics, and a tight pixel layout means significant coupling can occur.

Simulating the reset noise directly with an AC Noise analysis is complicated by the fact that the noise charge is stored on both the feedback capacitor and the input capacitor, and these two noises cannot be added in rms since they are partially correlated. The AC Noise analysis refers the total noise to only one pair of nodes in the circuit. To combine the charge noise from the two capacitors onto one pair of nodes, two auxiliary voltage controlled voltage sources (vcvs) are added to the simulation set-up. Figure 6 shows the simulation set-up; note the polarity of the connections to the controlled sources. With this simulation set-up, the reset noise can be directly measured from node Qt to ground. Integrating the results of an AC Noise sim over frequency with the reset switch closed gives the total reset noise when the reset switch is opened.
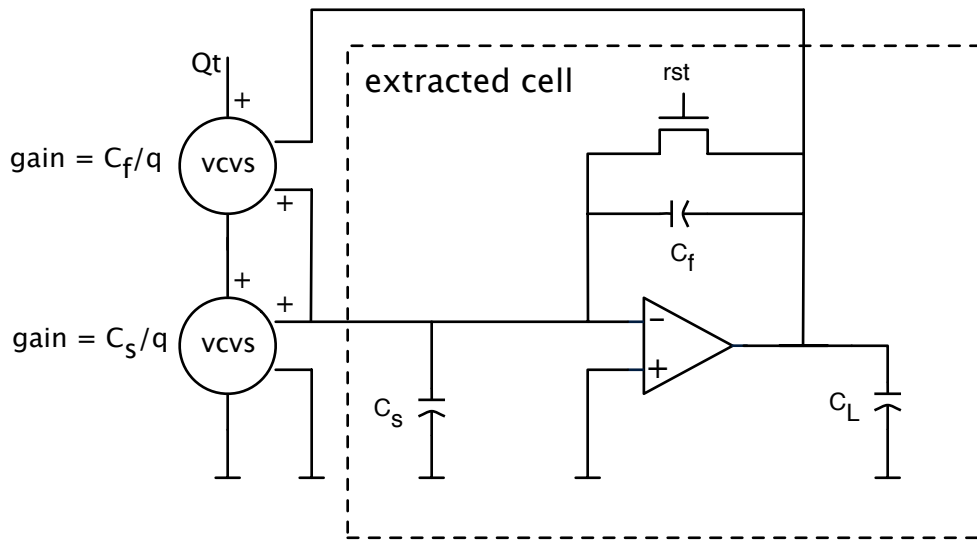

Figure 6 – Simulation set-up to measure the total charge left on the input node when the reset transistor turns off.

The gains of the controlled sources must be set to the input and feedback capacitances in the CTIA circuit to accurately model the charge. Since these capacitances consist of the intentional drawn values combined with parasitic values, a methodology is required to extract the total capacitances from simulation for annotation on the controlled sources. Looking into the input of the CTIA pixel in integration mode, the capacitance is:

$$C_1 = C_s + (1 + |A|)C_f \qquad (9)$$

|A| is the voltage gain of the amplifier, which can be directly measured as the ratio between the input voltage and output voltage of the CTIA amplifier. If, instead, the output of the CTIA amplifier is shorted to an AC ground, then the gain of the amplifier is zero and the capacitance looking into the pixel is:

$$C_2 = C_s + C_f \qquad (10)$$

To find C_f and C_s, an AC simulation is run in both conditions – first with the CTIA pixel in integration, and then with the CTIA amplifier shorted to an AC ground. Note that in both cases, the DC bias point for the AC simulation should be as if the CTIA has just been reset, as the parasitic capacitances of the amplifier depends on the biasing of the amplifier transistors. A replica CTIA can be used to create an AC ground with the right DC bias.

From these two capacitance measurements, along with the amplifier gain, the values of C_s and C_f can be determined. C_s and C_f contain the intentional capacitances, along with the parasitic capacitances due to the amplifier and extracted parasitics.

Using this methodology, AC Noise simulations were run on circuit in Figure 5 and the reset noise was measured and compared with the analytical results. Note that the CTIA pixel was designed to meet the assumption $R_{on}=1/g_m$, so that the results could be directly compared. The two results match within a few electrons, as shown in Figure 7.

Switched capacitor noise can also be simulated with SpectreRF, which is a tool that simulates noise folding in the frequency domain for circuits that translate frequency. SpectreRF first finds a periodic operating point for the circuit; then a noise analysis can be run over the baseband frequency to evaluate the amount of high frequency noise that folds down into the baseband frequency.[6]

SpectreRF becomes extremely computationally intensive when the ratio of the maximum noise frequency to the sampling frequency is high; this is referred to in SpectreRF as the number of sidebands. Unfortunately, the number of sidebands for accurate noise results is typically very large for CTIA pixels. This is because CTIA pixels are slow to settle due to their limited g_m and low feedback factors, but contain very high frequency noise due to the small capacitances involved. For the circuit in Figure 5, a periodic simulation time of 10 usec was used with 5000 sidebands, to include noise components up to 500 MHz, and the number of frequency points for the noise analysis was limited to keep the simulation time reasonable. The results are also plotted in Figure 7, and are slightly higher than the results from the AC Noise sim. This may be due to inaccurate interpolation between the limited noise frequency points past the 1/f knee frequency.
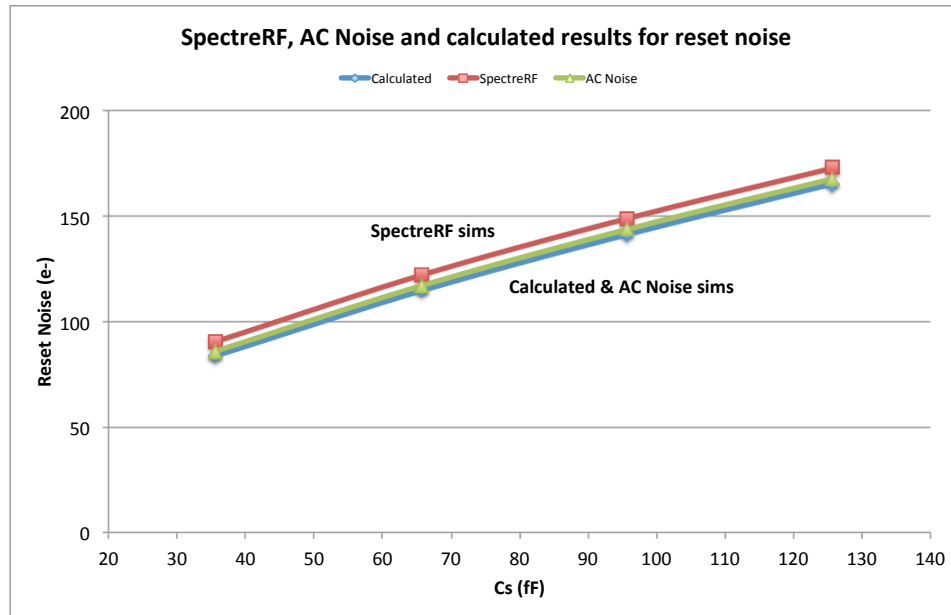

Figure 7 – Comparison of the reset noise results obtained from simulation using SpectreRF, AC Noise with the test circuit shown in Figure 6, and calculations from the presented analysis. Cs was varied, while Cf = 5fF and CL = 400fF.

Another more direct simulation for sampled noise is the transient noise simulation. In this simulation, a standard time-domain simulation is performed, with the addition of injected transient device noise. The injected noises are updated with a time interval that captures the highest noise frequency of interest, and are randomized to simulate the noise PSD of that particular devices noise. For the CTIA reset noise, each transient noise simulation provides one data point for the reset noise distribution. By running the transient noise simulation multiple times, a histogram can be created of the reset noise distribution and the standard deviation can be measured.

Results of 300 transient noise simulations are shown in Figure 8 and Figure 9, for the case where Cs=125fF on Figure 7. The standard deviation of the noise distribution histogram yields 177 e-. This matches the other approaches to simulating the reset noise. However, transient noise simulations are also very computationally expensive, due to the small time steps required to model high frequency noise, and the multiple simulations required to create the sampled noise histogram.
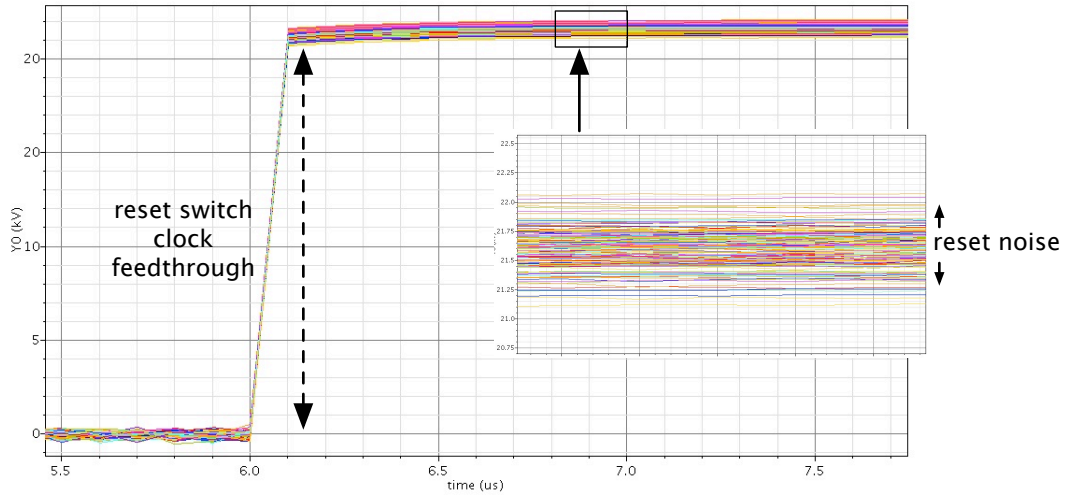
Figure 8 – Simulation results of multiple transient noise sims on the CTIA based pixel, in this case with C_f=5fF, C_L=400fF, and C_s=125fF. The reset switch clock feed-through introduces a large constant pedestal, and the reset noise is the variation in the final charge at the CTIA input node when the reset switch opens.
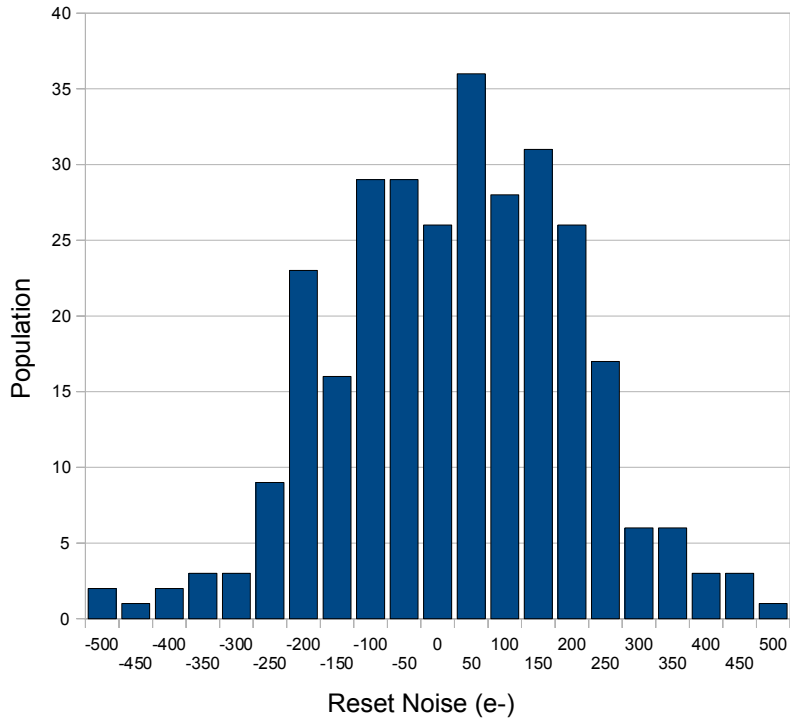

Figure 9 – Histogram of the final reset noise values from 300 transient noise simulation runs, for the case shown in Figure 8. The standard deviation is found to be 177 e-, which matches the results from the other simulations and the analysis.

Table 1 compares the three different approaches to simulating the CTIA pixel reset noise. The AC Noise simulation set-up is complicated by the requirement that the capacitances be extracted and back-annotated onto auxiliary controlled sources in the circuit. Once this has been accomplished, running the simulation is fast, and the results do not require further post-processing.

SpectreRF is much more complicated to set-up and run. The simulation set-up requires that the periodic operating condition be chosen carefully, to limit the number of sidebands that will be needed. Important settings that determine the accuracy must be refined through trial and error. The simulation itself takes much longer than the AC Noise analysis for the large number of sidebands needed, even for a much coarser sampling of frequency points.

The transient noise simulation is the easiest to set-up, but it requires a careful choice of the maximum noise frequency, as this trades off simulation speed for accuracy. The simulation time is long due to the small time-steps used to model high frequency noise, and many simulations must be run to accumulate enough data points to accurately calculate the noise statistics.

A powerful feature of SpectreRF and transient noise simulations is that they are able to model non-linear effects, whereas the AC Noise simulation cannot. Using all three analyses is useful to double-check the reset noise results, but the AC Noise simulation is most appropriate for the repeated analysis typical during the initial design and layout phase. On the other hand, if the simulation times can be reduced, the transient noise simulation provides the most intuitive results and requires less detailed knowledge about the circuit.

Simulation Analysis	Type	Simulation Set-up	Simulation Settings	Simulation time	Results analysis	Non-linear effects
AC Noise	Frequency-domain	Moderate	Easy	Short	Simple	No
SpectreRF	Frequency-domain	Moderate	Difficult	Long	Moderate	Yes
Transient Noise	Time-domain	Easy	Moderate	Long	Complicated	Yes

Table 1 – Comparison of simulation analyses for switched-capacitor noise.

5. CONCLUSION

This paper has presented an analysis and simulation methodology for predicting the reset noise from CTIA based pixels. The reset noise is an important characteristic of CTIA pixels. It can be removed effectively with CDS, at the expense of the additional complexity of a frame memory and with a doubling of the readout bandwidth. To determine the improvement provided by CDS requires comparing the reset noise with the noise levels of the rest of the system and the readout speed/noise tradeoffs. Lowering the reset noise with a bandwidth limiting capacitor at the output of the CTIA is limited in its application and requires longer reset times for the circuit to settle. However, decreasing the detector capacitance is very effective in reducing the reset noise.

Simulating the reset noise can be accomplished with a Spice AC Noise sim, with the addition of controlled sources to model the noise charge on the input of the CTIA when the reset switch opens. This approach was compared with SpectreRF and transient noise simulations, and all three give similar results. However, SpectreRF and transient noise are both computationally intensive, reducing their suitability for repeated analysis during the design process.

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